EEC2146: Electronic Circuits and Measurements

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EEC2146: Electronic Circuits and Measurements

LEC: 2
Review On FET Transistor

FET Transistors

Objectives and outline:

1. Structure of FET transistors
2. Basic operation
3. Modes of operation
5. I-V characteristics of A practical FET
6. DC analysis
7. Small signal model of FET
8. AC analysis of FET Amplifiers

FET Transistors

Comparison between BJT and FET

Similarities:

Amplifiers.
Switching devices.
Impedance matching circuits.

Differences:

FETs are voltage controlled devices. BJTs are current controlled devices.

FETs have higher input impedance. BJTs have higher gain.

FETs are less sensitive to temperature variations and are better suited for integrated circuits

FETs are generally more static sensitive than BJTs.

FET Transistors

Types of FET

- Types of FET
  - JFET
    - p-channel
    - n-channel
  - MOSFET
    - p-channel
      - enhancement
      - depletion
    - n-channel
      - enhancement
      - depletion

FET Transistors

JFET (N-Channel)

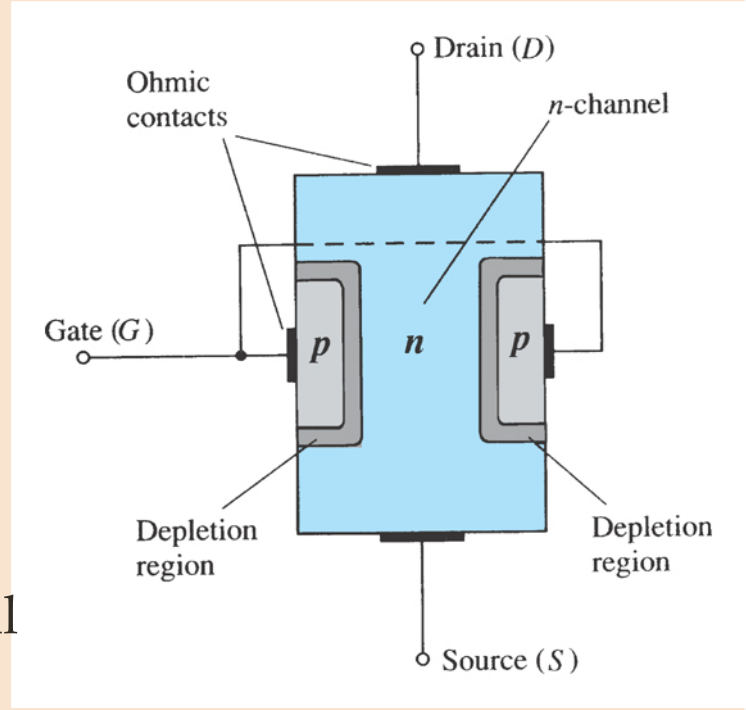
There are two types of JFETs:

***n*-channel**
***p*-channel**

JFETs have three terminals:

The **Drain** (D) and **Source** (S) are connected to the *n*-channel

The **Gate** (G) is connected to the *p*-type material



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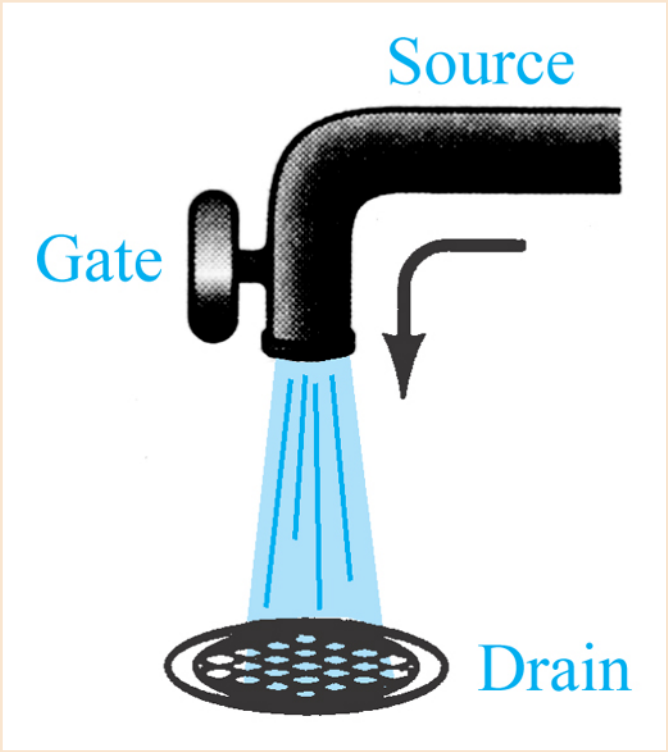
JFET (N-Channel)

The source is the accumulation of electrons at the negative pole of the drain-source voltage.

The drain is the electron deficiency (or holes) at the positive pole of the applied voltage.

The gate controls the width of the n-channel and, therefore, the flow of charges from source to drain.



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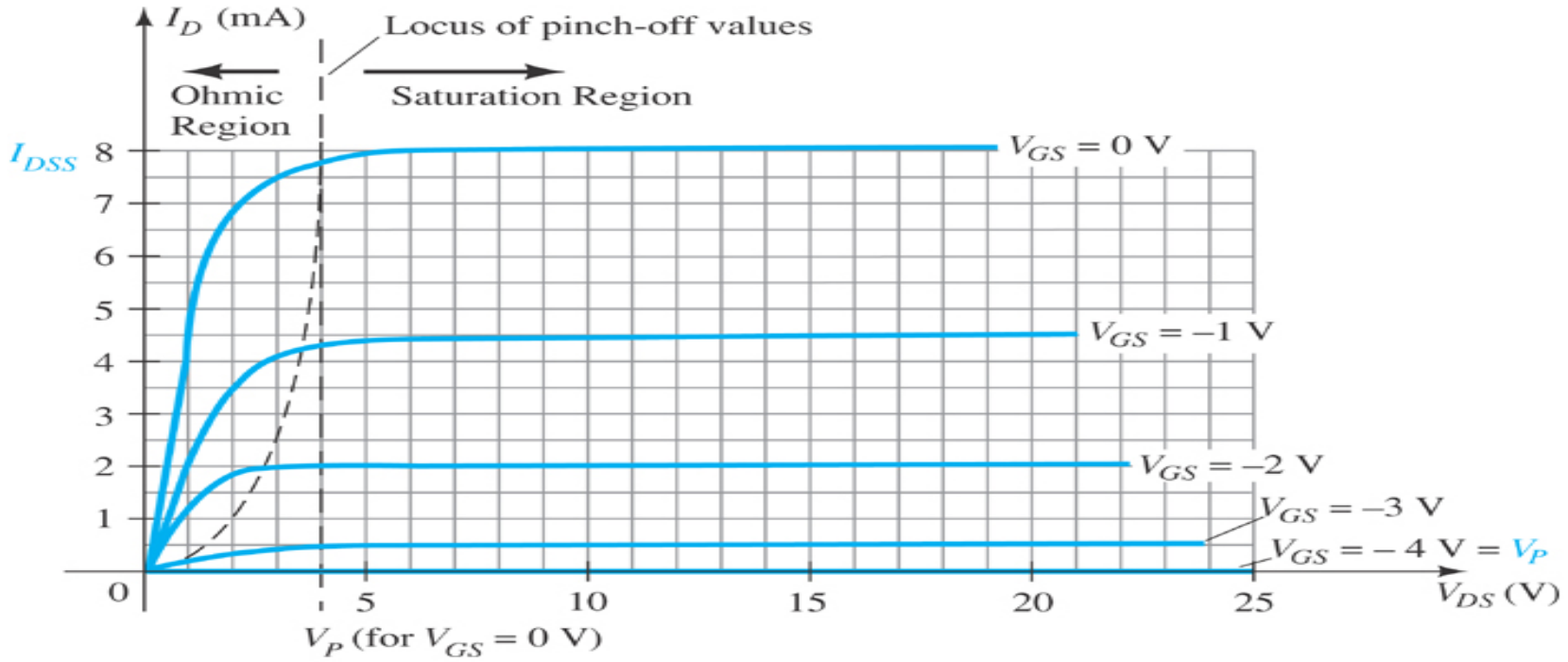
JFET (N-Channel)

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$



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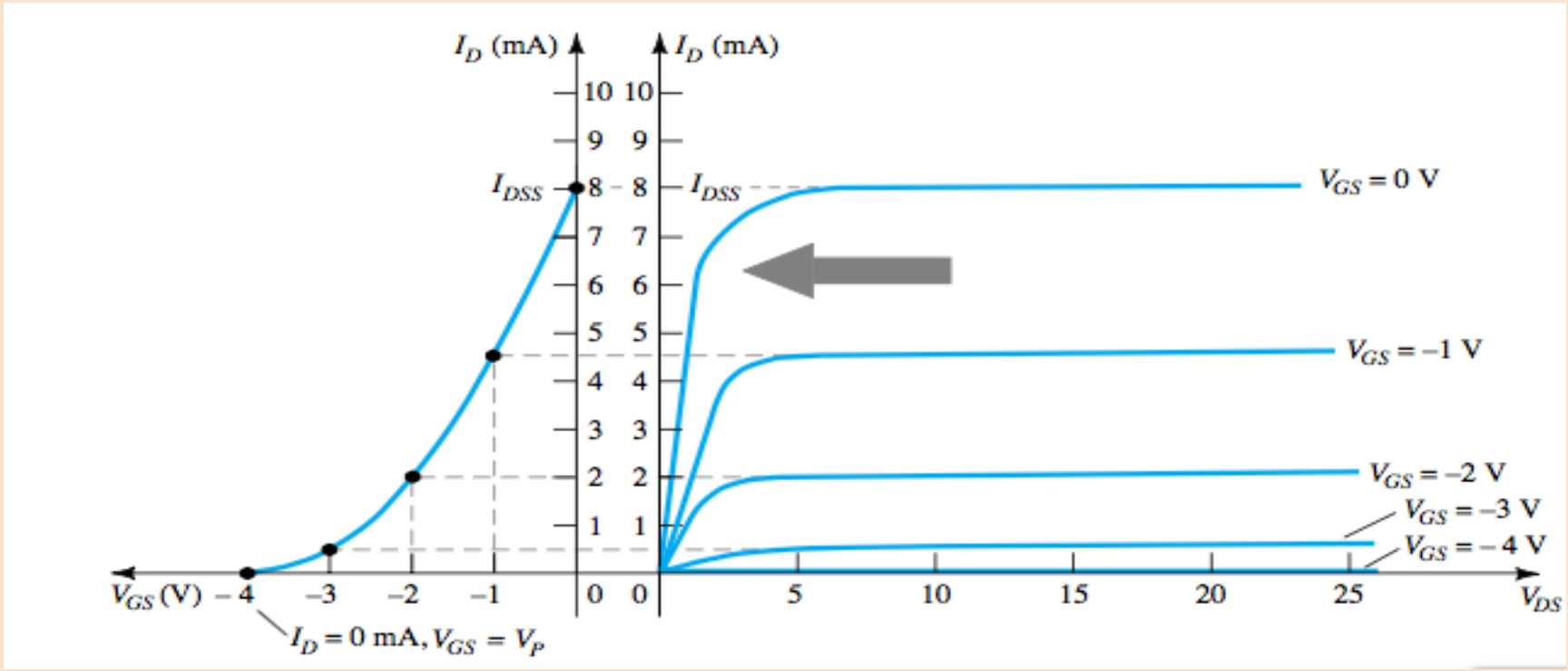
JFET (N-Channel)

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$



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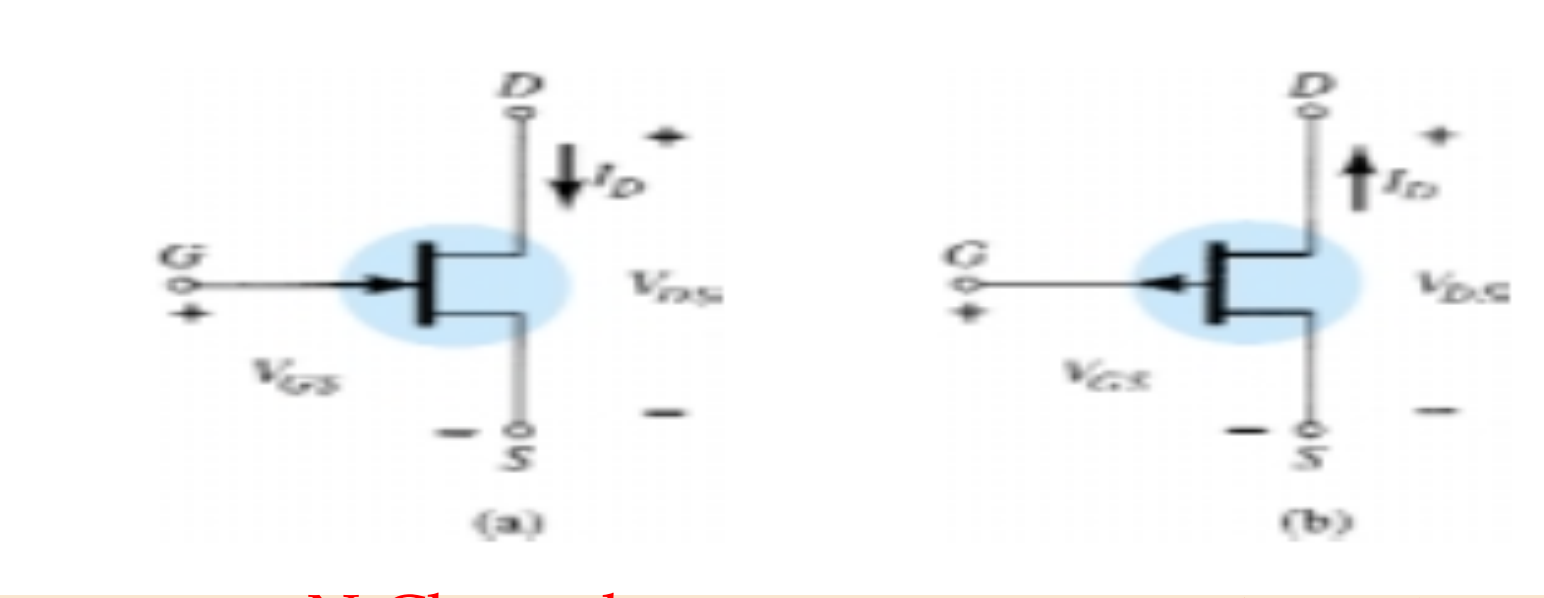
Important Relations

JFET		BJT
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$\Leftrightarrow$	$I_C = \beta I_B$
$I_D = I_S$	$\Leftrightarrow$	$I_C \cong I_E$
$I_G \cong 0\ \text{A}$	$\Leftrightarrow$	$V_{BE} \cong 0.7\ \text{V}$

FET Transistors

JFET Symbols



N-Channel

P-Channel

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FET Transistors

MOSFET

MOSFETs have characteristics similar to those of JFETs and additional characteristics that make then very useful.

There are two types of MOSFETs:

Depletion-Type

Enhancement-Type

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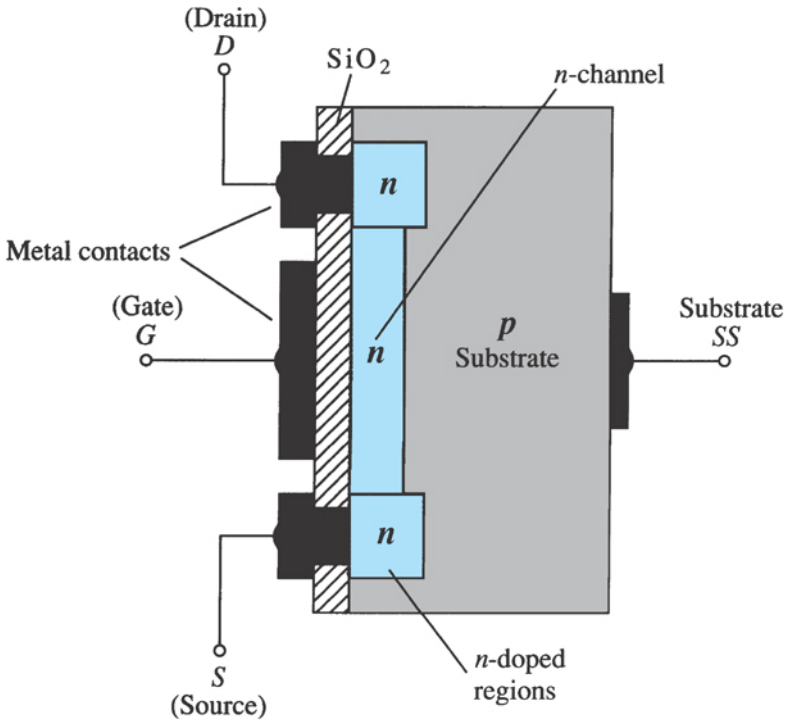
FET Transistors

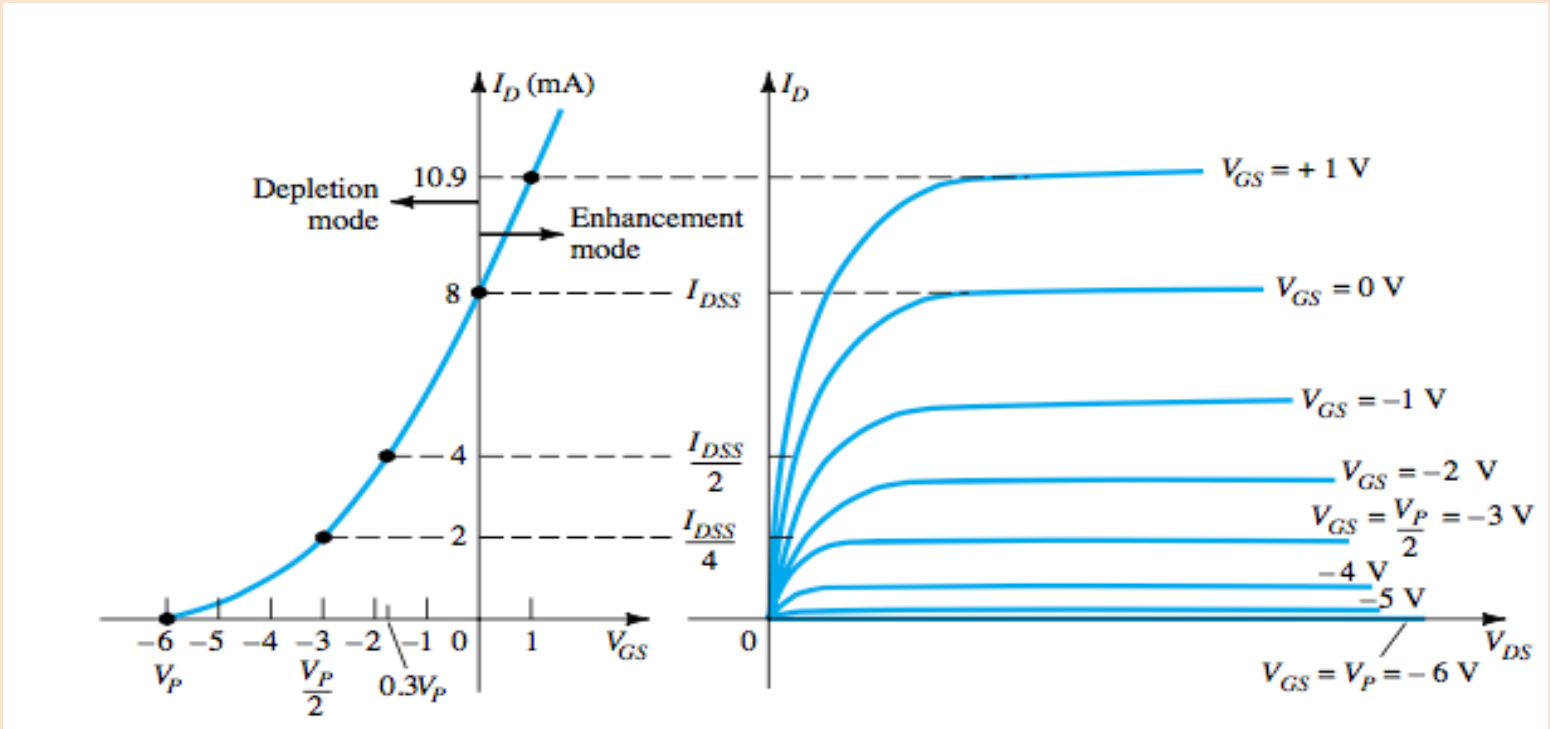
MOSFET (Depletion type)

The **Drain** (D) and **Source** (S) connect to the to *n*-type regions. These *n*-typed regions are connected via an *n*-channel. This *n*-channel is connected to the **Gate** (G) via a thin insulating layer of silicon dioxide (SiO_2). The *n*-type material lies on a *p*-type substrate that may have an additional terminal connection called the **Substrate** (SS).



FET Transistors

MOSFET (Depletion type)



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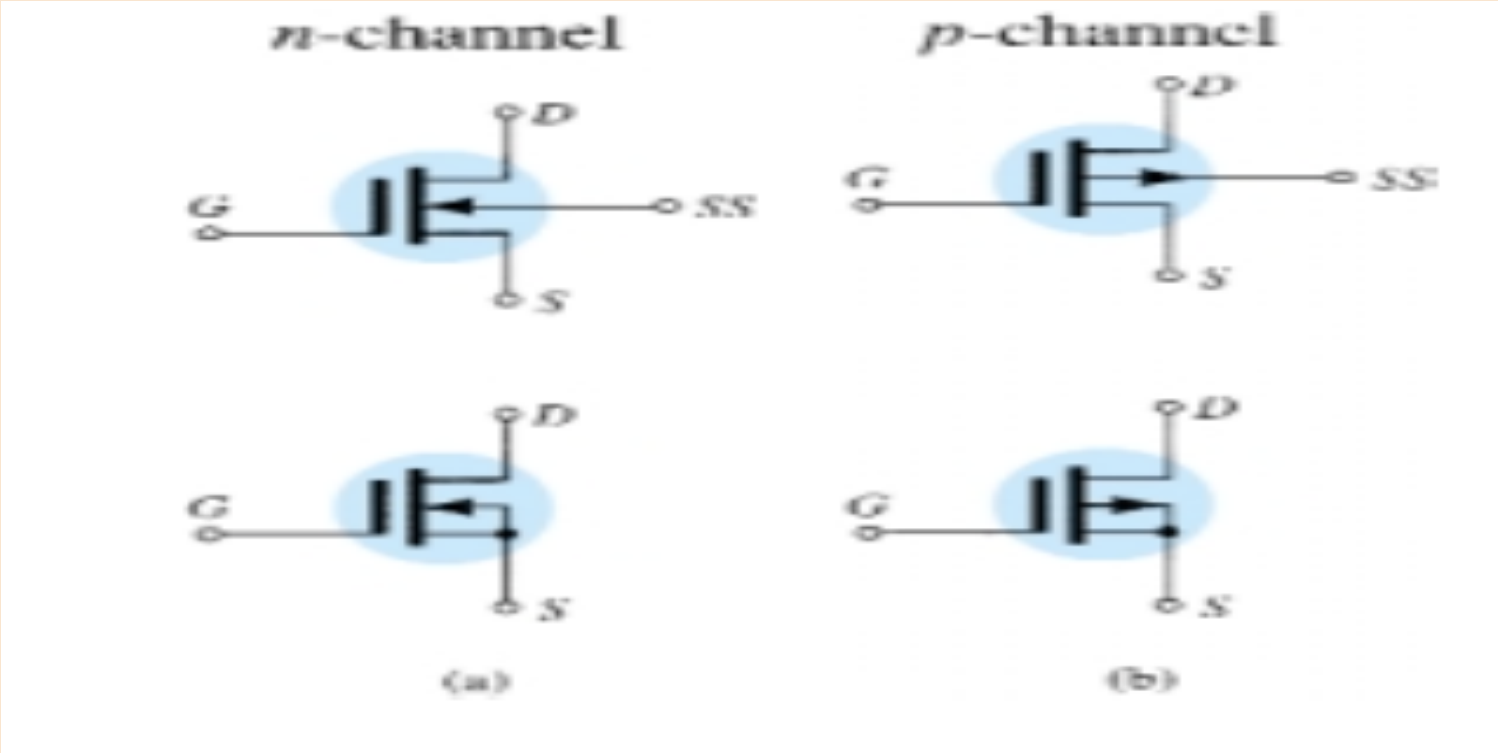
MOSFET (Depletion type)

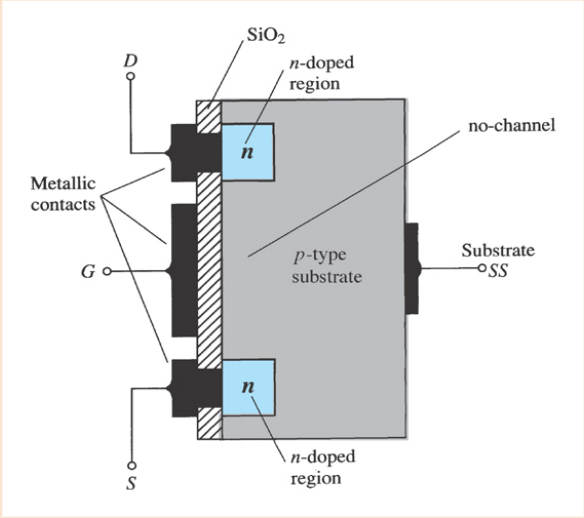


FET Transistors

MOSFET (Enhancement type)

The **Drain (D)** and **Source (S)** connect to the to *n*-type regions. These *n*-type regions are connected via an *n*-channel

- The **Gate (G)** connects to the *p*-type substrate via a thin insulating layer of silicon dioxide (SiO_2)
- There is no channel
- The *n*-type material lies on a *p*-type substrate that may have an additional terminal connection called the **Substrate (SS)**



FET Transistors

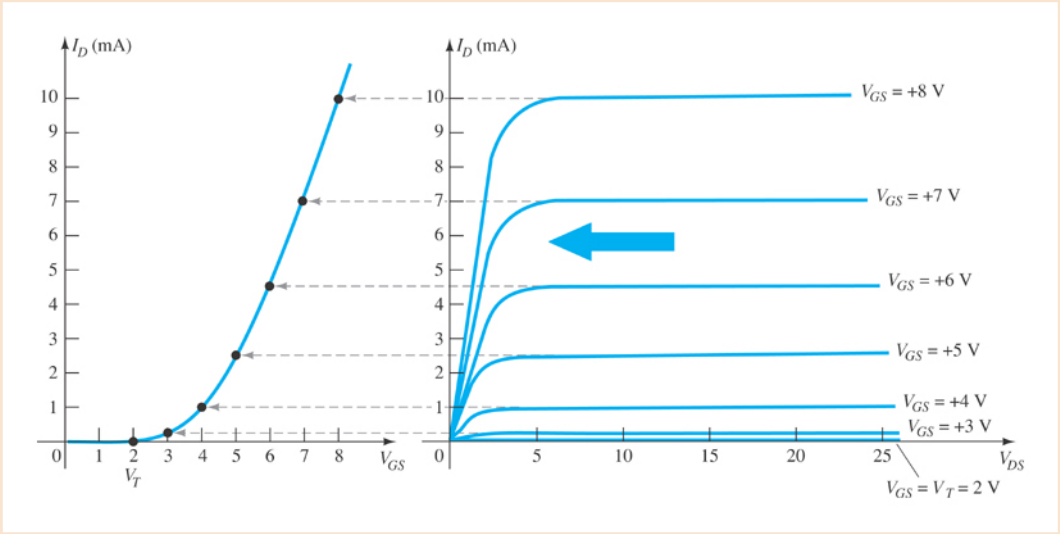
MOSFET (Enhancement type)

The enhancement-type MOSFET (E-MOSFET) operates only in the enhancement mode.

V_{GS} is always positive

As V_{GS} increases, I_D increases

As V_{GS} is kept constant and V_{DS} is increased, then I_D saturates (I_{DSS}) and the saturation level (V_{DSsat}) is reached



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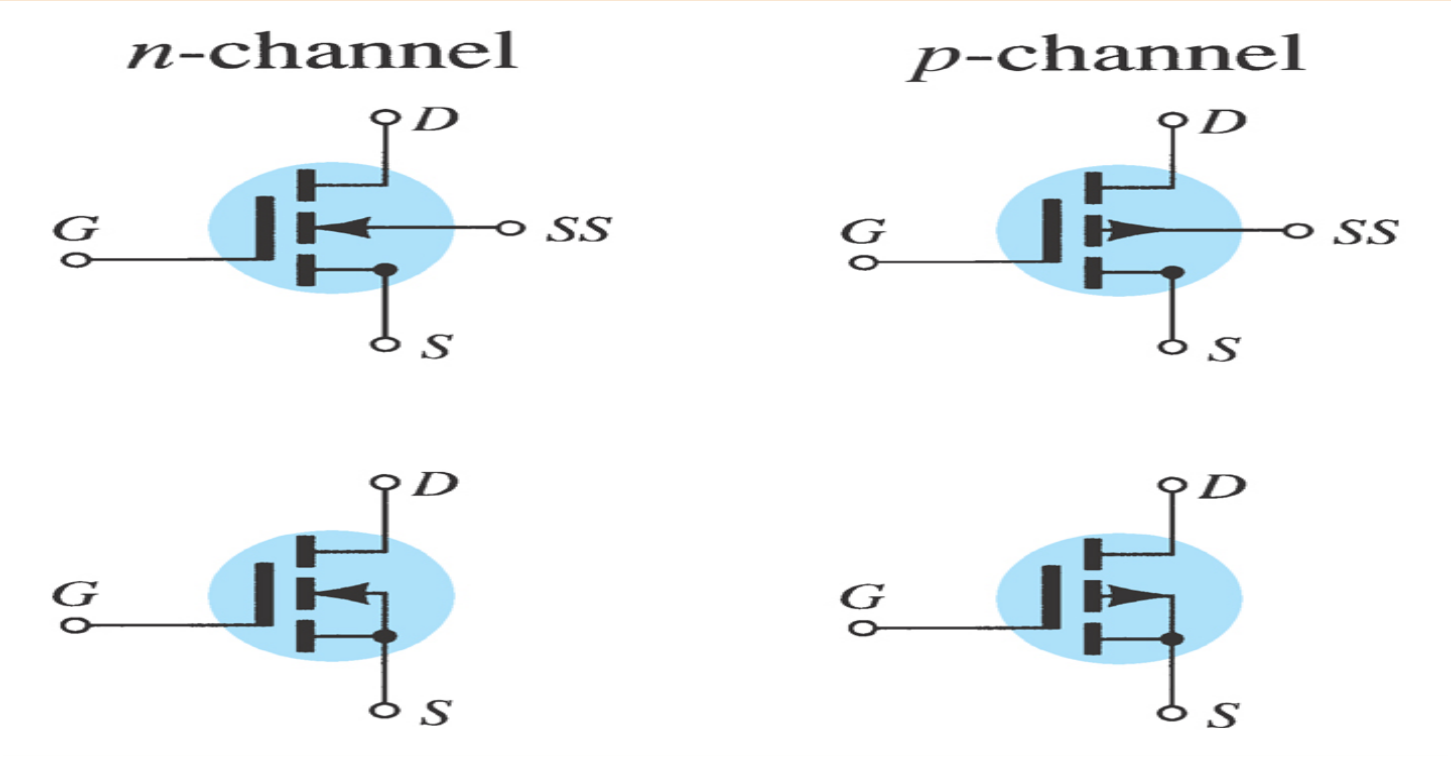
MOSFET (Enhancement type)



FET Transistors

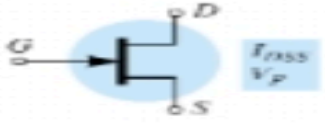
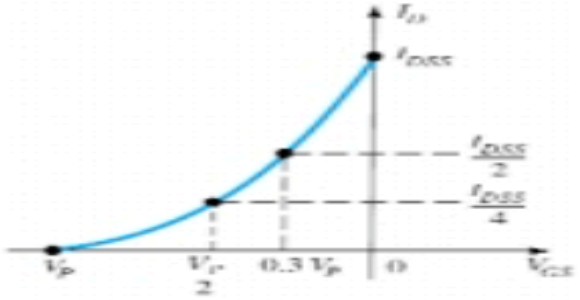
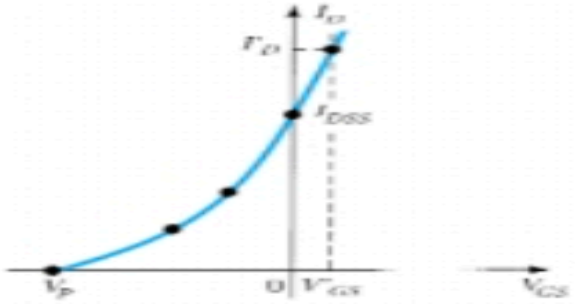
Important Relations

$$I_D = k(V_{GS} - V_T)^2$$

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

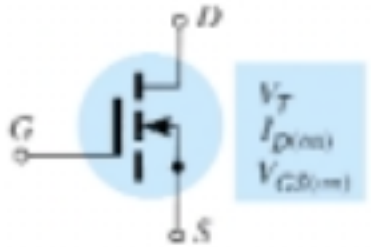
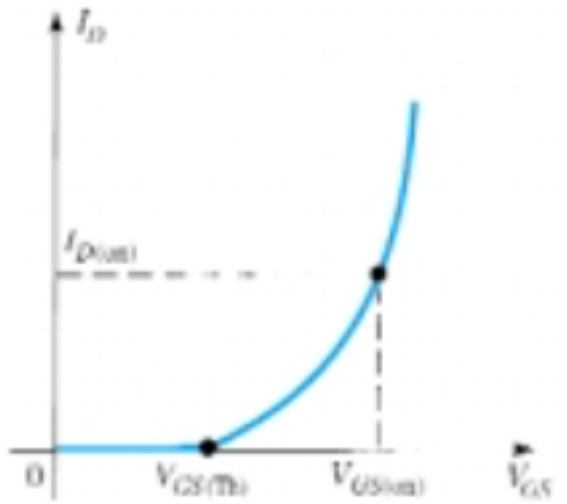
FET Transistors

Summary:

Type	-Symbol- Basic Relationships	Transfer Curve
JFET (*n*-channel)	$I_G = 0\text{ A}, I_D = I_S$  $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	
MOSFET depletion-type (*n*-channel)	$I_G = 0\text{ A}, I_D = I_S$  $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	

FET Transistors

Summary:

MOSFET enhancement-type (*n*-channel)	$I_G = 0\ \text{A}, I_D = I_S$  $I_D = k(V_{GS} - V_{GS(Th)})^2$ $k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$	

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FET Transistors

DC Analysis

$$I_G \cong 0\ \text{A}$$

$$I_D = I_S$$

$$I_D = I_{DSS}\left(\frac{1 - V_{GS}}{V_P}\right)^2$$

$$I_D = k(V_{GS} - V_T)^2$$

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FET Transistors

DC Analysis (Fixed Bias)

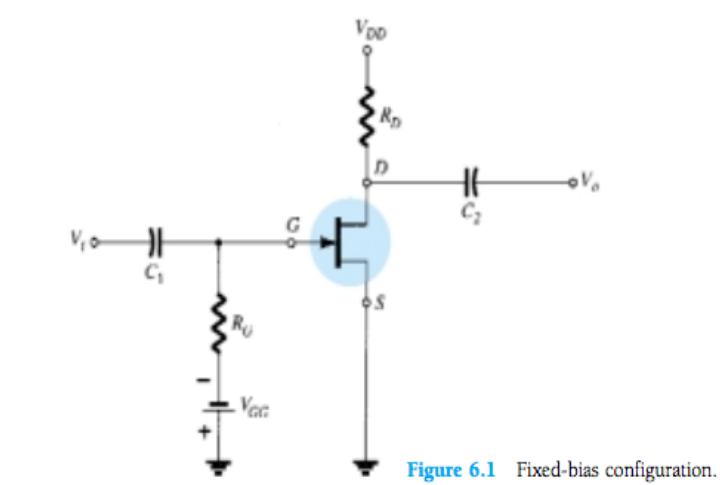

Figure 6.1 Fixed-bias configuration.

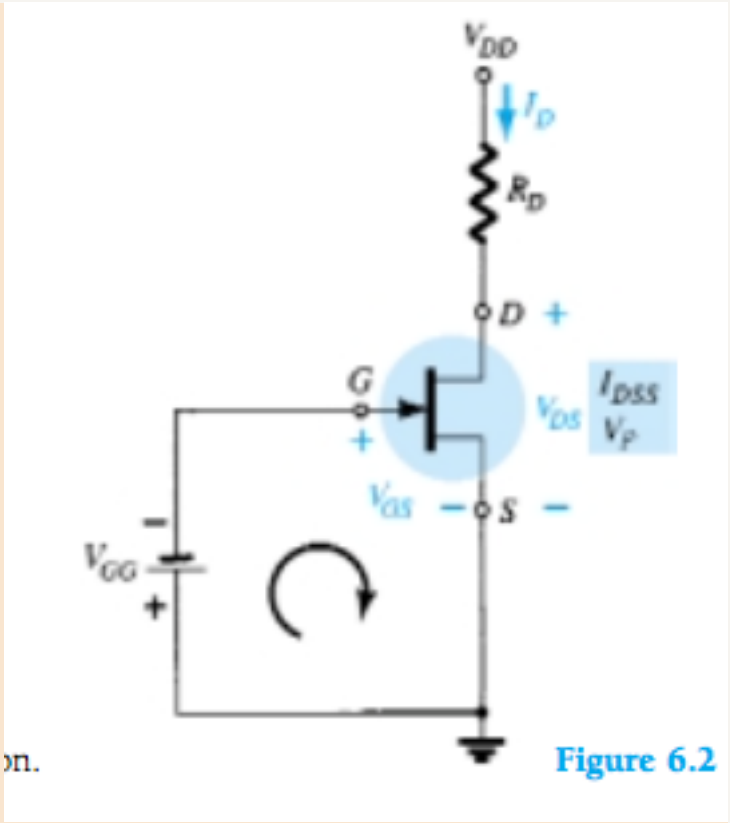

Figure 6.2

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FET Transistors

DC Analysis (Fixed Bias)

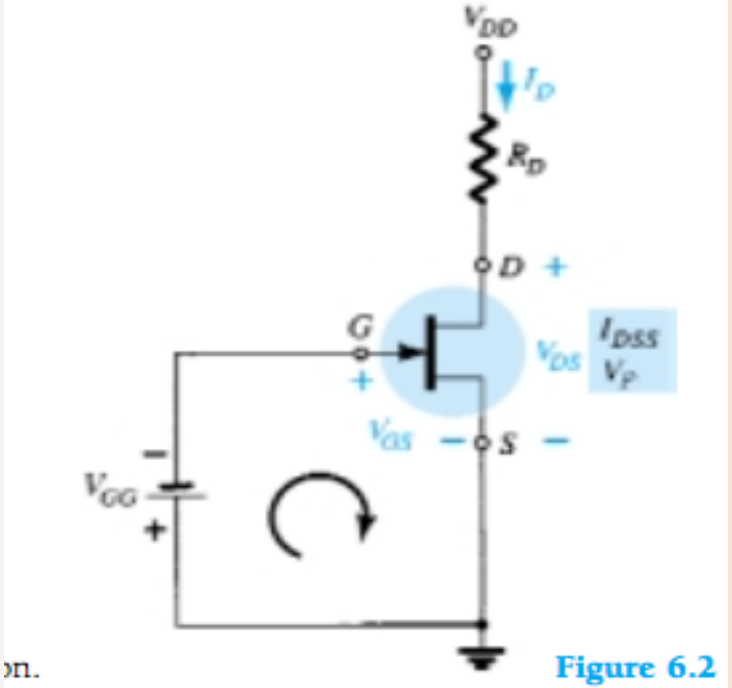

Figure 6.2

$$-V_{GG} - V_{GS} = 0$$

$$V_{GS} = -V_{GG}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$+V_{DS} + I_D R_D - V_{DD} = 0$$

$$V_{DS} = V_{DD} - I_D R_D$$

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DC Analysis (Fixed Bias)

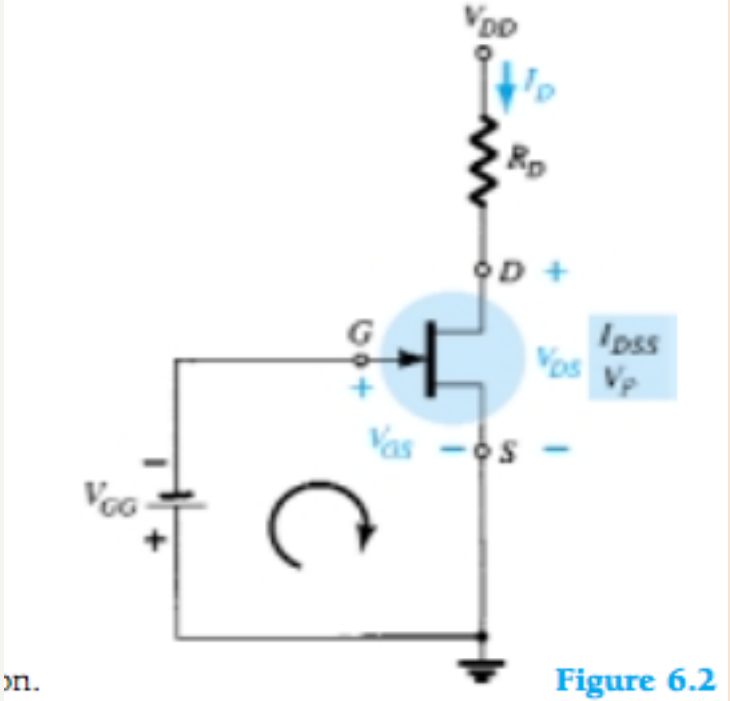

Figure 6.2

$$V_S = 0\ \text{V}$$

$$V_D = V_{DS}$$

$$V_G = V_{GS}$$

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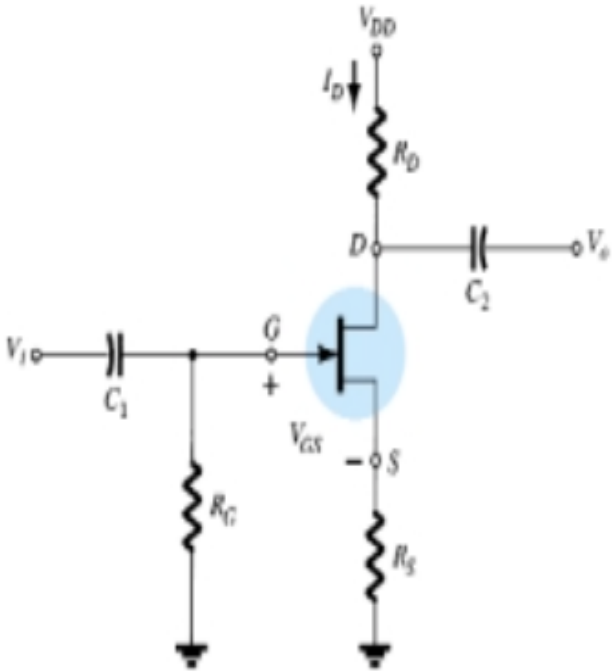
FET Transistors

DC Analysis (Self Bias)



$$V_{GS} = -I_D R_S$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{-I_D R_S}{V_P}\right)^2$$

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

$$I_D^2 + K_1 I_D + K_2 = 0$$

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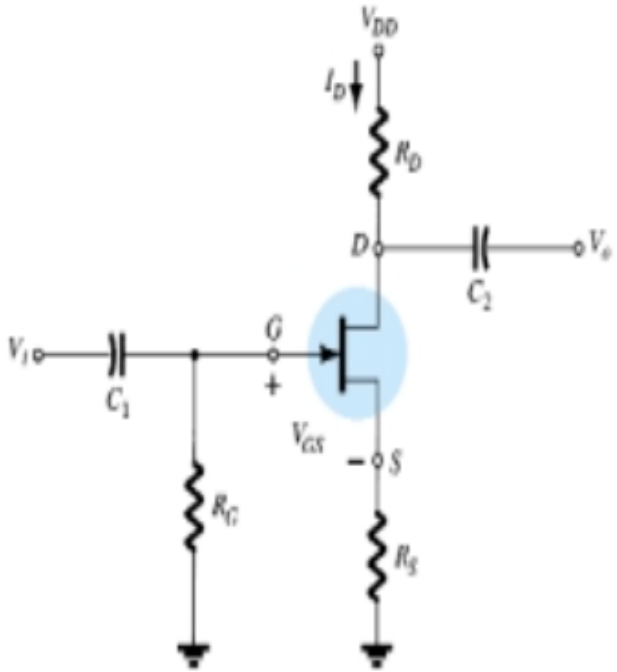
DC Analysis (Self Bias)



$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

$$V_S = I_D R_S$$

$$V_G = 0\ \text{V}$$

$$V_D = V_{DS} + V_S = V_{DD} - V_{R_D}$$

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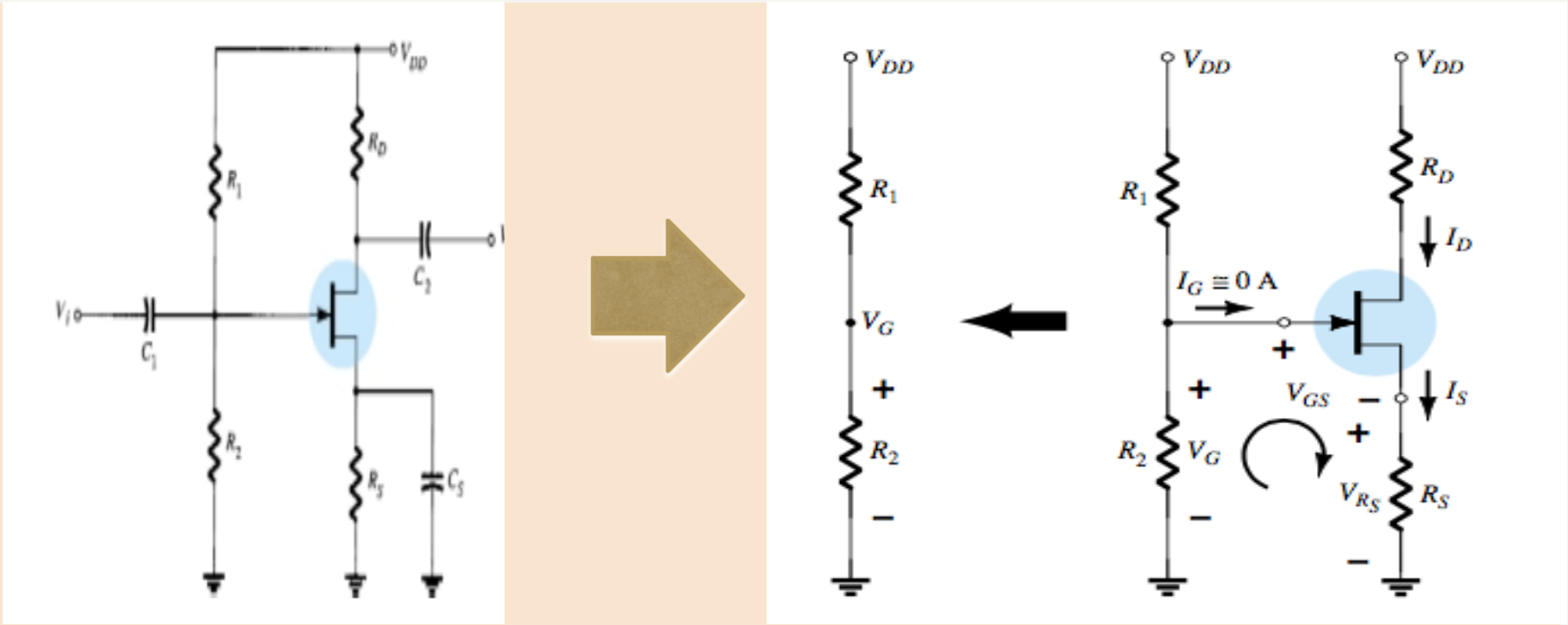
FET Transistors

DC Analysis (Voltage Divider)



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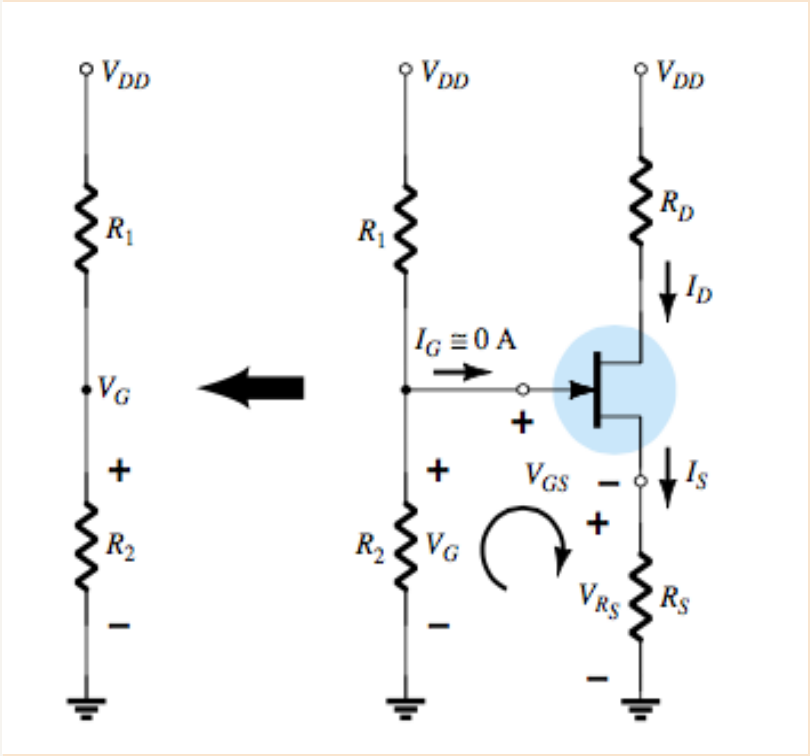
DC Analysis (Voltage Divider)



$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_G - V_{GS} - V_{R_S} = 0$$

$$V_{GS} = V_G - V_{R_S}$$

$$V_{GS} = V_G - I_D R_S$$

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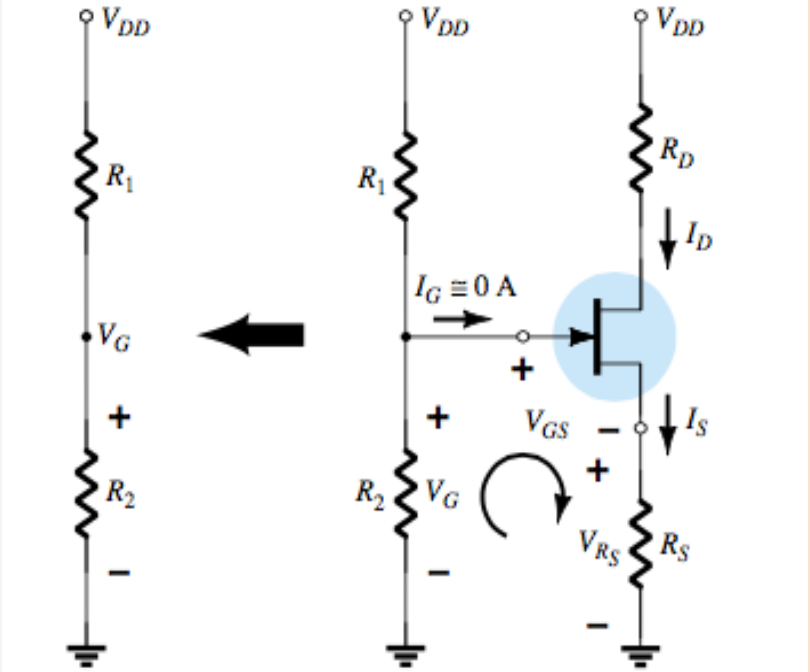
FET Transistors

DC Analysis (Voltage Divider)



$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$V_D = V_{DD} - I_D R_D$$

$$V_S = I_D R_S$$

$$I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}$$

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DC Analysis (Depletion MOSFET)

The similarities in appearance between the transfer curves of JFETs and depletion- type MOSFETs permit a similar analysis of each in the dc domain. The primary difference between the two is the fact that depletion-type MOSFETs permit operating points with positive values of V_{GS} and levels of I_D that exceed I_{DSS}. In fact, for all the configurations discussed thus far, the analysis is the same if the JFET is replaced by a depletion-type MOSFET.

FET Transistors

DC Analysis (Enhancement MOSFET)

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$

$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$

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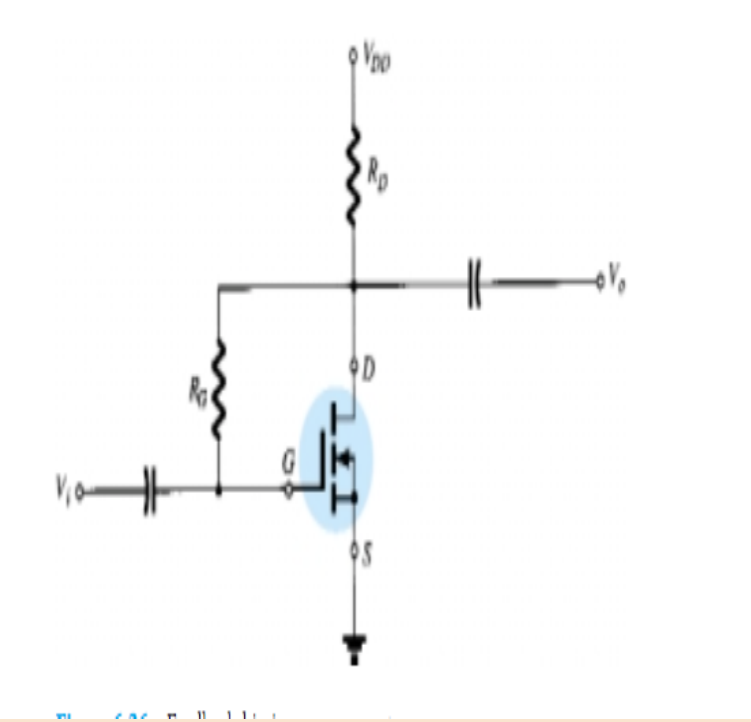
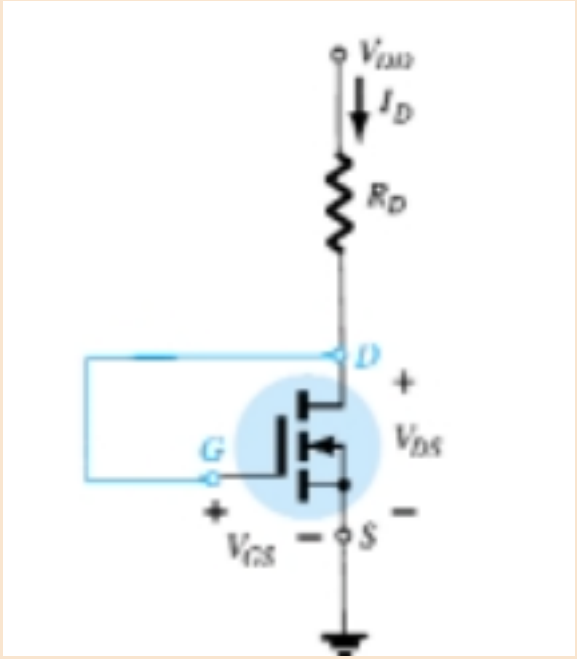
FET Transistors

DC Analysis (Enhancement MOSFET)





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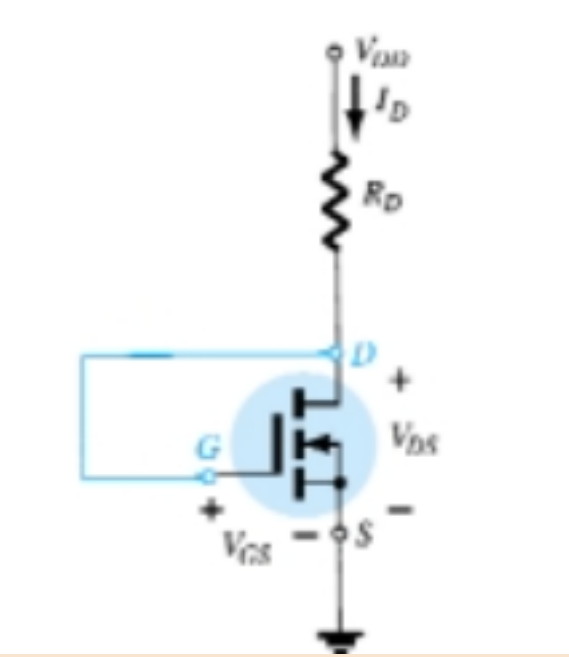
DC Analysis (Enhancement MOSFET)



$$V_D = V_G$$

$$\boxed{V_{DS} = V_{GS}}$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$\boxed{V_{GS} = V_{DD} - I_D R_D}$$

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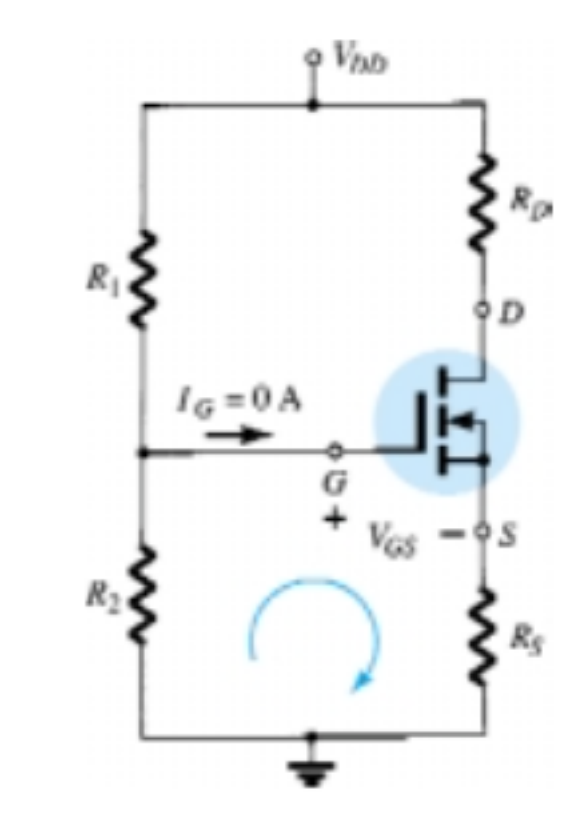
FET Transistors

DC Analysis (Voltage Divider)



$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$+V_G - V_{GS} - V_{R_S} = 0$$

$$V_{GS} = V_G - V_{R_S}$$

$$V_{GS} = V_G - I_D R_S$$

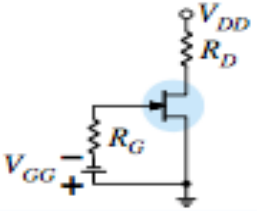
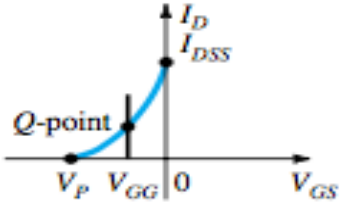
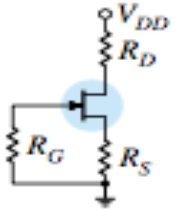
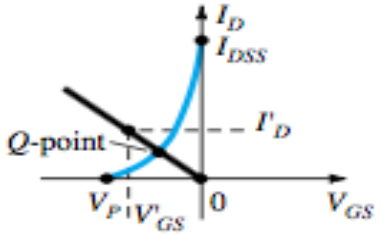
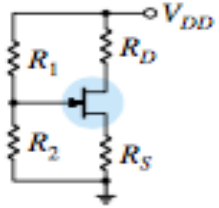
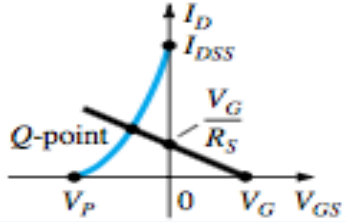
$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D}$$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

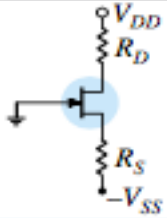
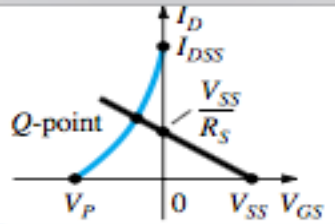
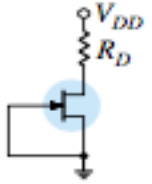
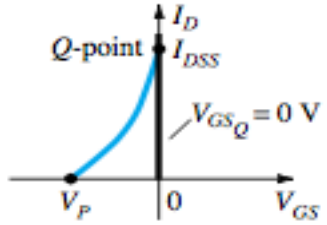
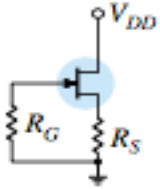
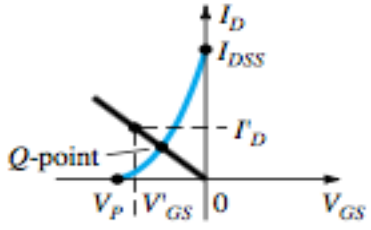
FET Transistors

DC Analysis (Summary)

Type	Configuration	Pertinent Equations	Graphical Solution
JFET Fixed-bias		$V_{GSQ} = -V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
JFET Self-bias		$V_{GS} = -I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	

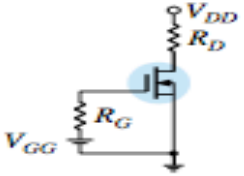
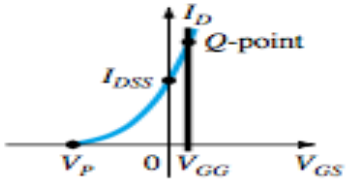
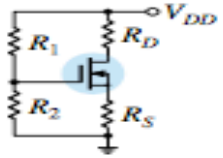
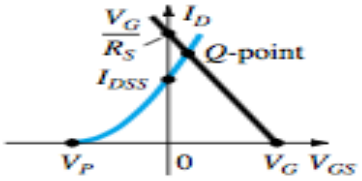
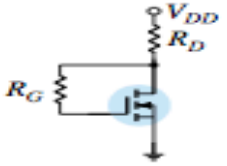
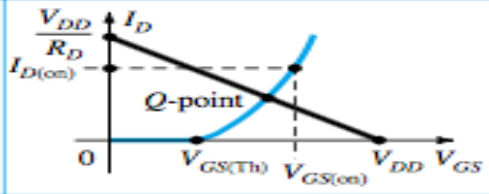
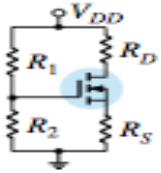
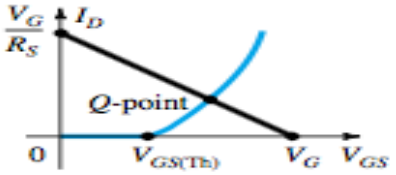
FET Transistors

DC Analysis (Summary)

JFET Common-gate		$V_{GS} = V_{SS} - I_D R_S$ $V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)$	
JFET ($V_{GSQ} = 0$ V)		$V_{GSQ} = 0$ V $I_{DQ} = I_{DSS}$	
JFET ($R_D = 0\ \Omega$)		$V_{GS} = -I_D R_S$ $V_D = V_{DD}$ $V_S = I_D R_S$ $V_{DS} = V_{DD} - I_S R_S$	

FET Transistors

DC Analysis (Summary)

Depletion-type MOSFET Fixed-bias		$V_{GSQ} = +V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
Depletion-type MOSFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_S R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
Enhancement type MOSFET Feedback configuration		$V_{GS} = V_{DS}$ $V_{GS} = V_{DD} - I_D R_D$	
Enhancement-type MOSFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$	

Break

FET Transistors

AC Analysis:

FETs provide:

- Excellent voltage gain
- High input impedance
- Low-power consumption
- Good frequency response

FET Transistors

AC Analysis:

Transconductance: The ratio of a change in I_D to the corresponding change in V_{GS}

- Transconductance is denoted g_m and given by:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

FET Transistors

Mathematical Definitions of g_m

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]$$

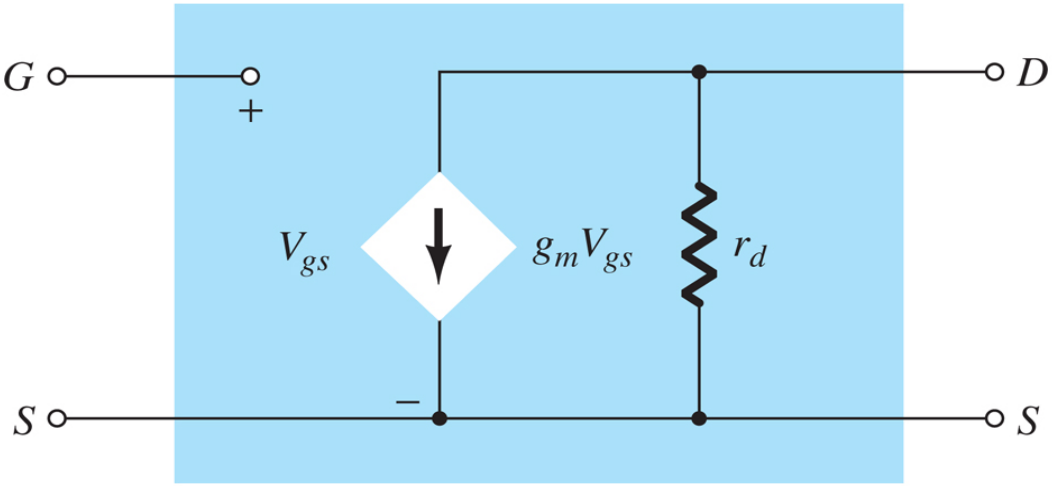
For $V_{GS} = 0$ V

$$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}$$

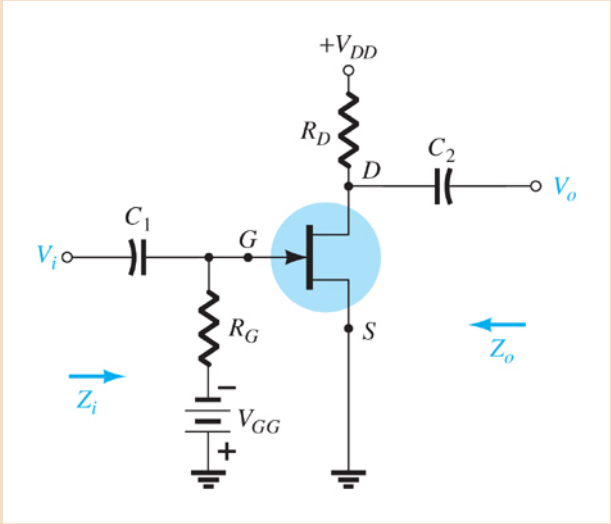
FET Transistors

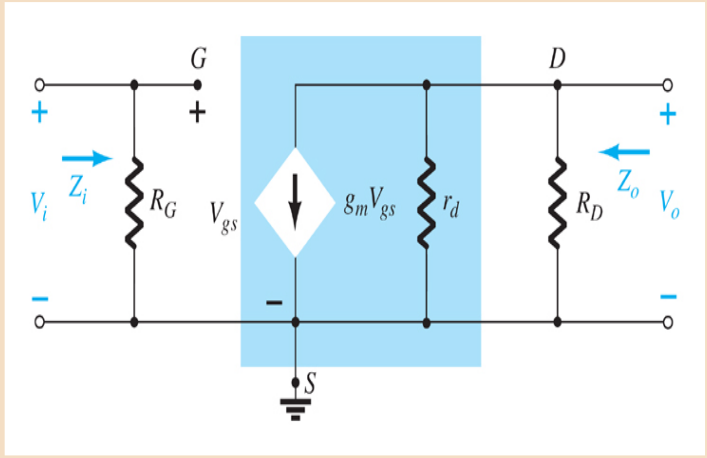
FET AC Equivalent Circuit



FET Transistors

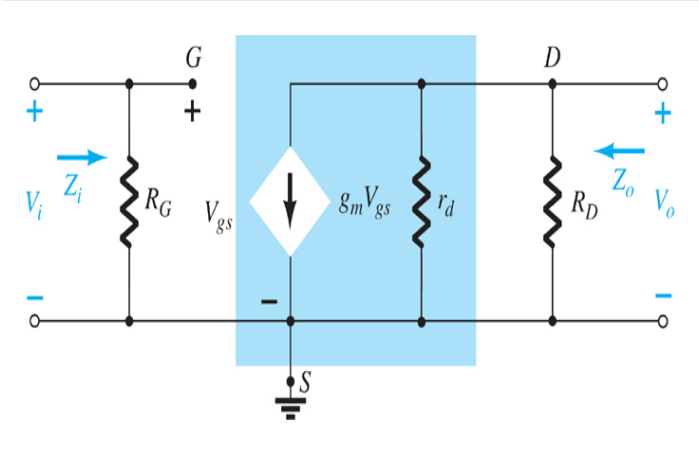
Common-Source (CS) Fixed-Bias





FET Transistors

Common-Source (CS) Fixed-Bias



Input impedance:

$$Z_i = R_G$$

$$Z_o = R_D \| r_d$$

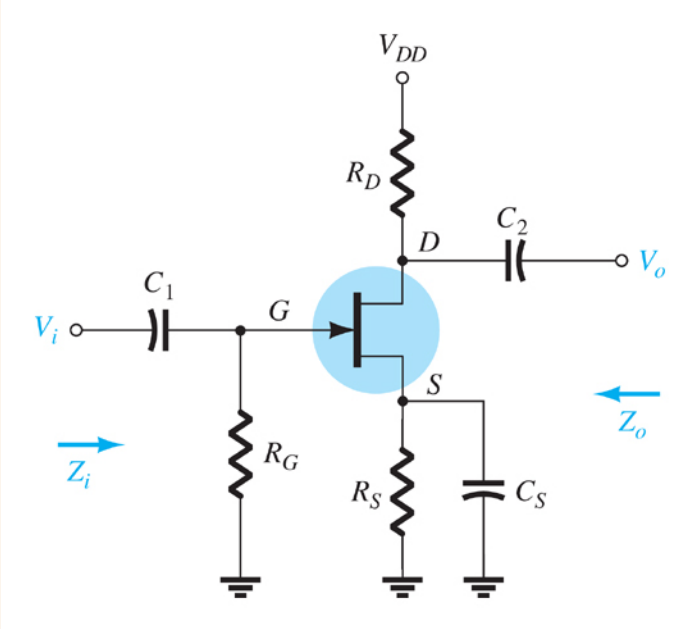
$$Z_o \cong R_D \Big|_{r_d \geq 10 R_D}$$

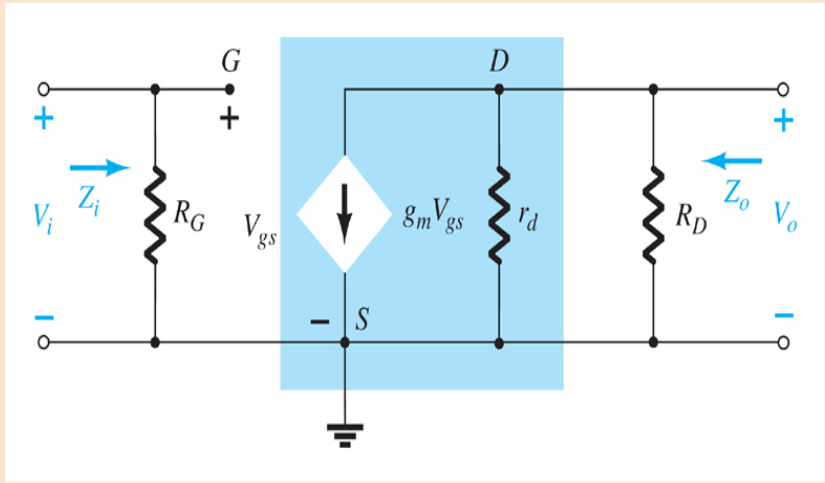
$$A_v = \frac{V_o}{V_i} = -g_m (r_d \| R_D)$$

$$A_v = \frac{V_o}{V_i} = -g_m R_D \Big|_{r_d \geq 10 R_D}$$

FET Transistors

AC Analysis (self bias)





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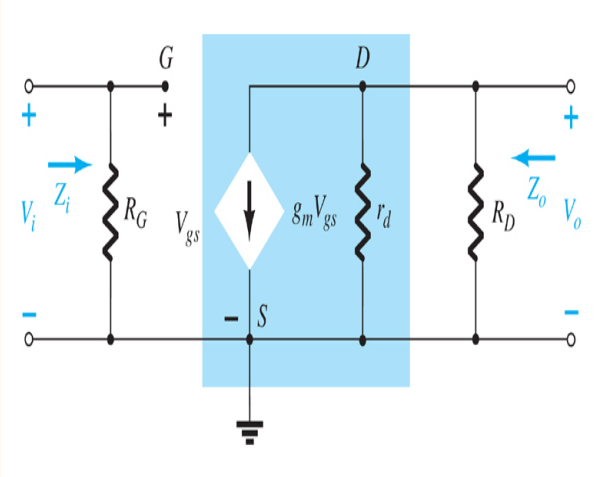
FET Transistors

AC Analysis (self bias)



$$Z_i = R_G$$

$$Z_o = r_d \| R_D$$

$$Z_o \cong R_D \Big|_{r_d \geq 10 R_D}$$

$$A_v = -g_m (r_d \| R_D)$$

$$A_v = -g_m R_D \Big|_{r_d \geq 10 R_D}$$

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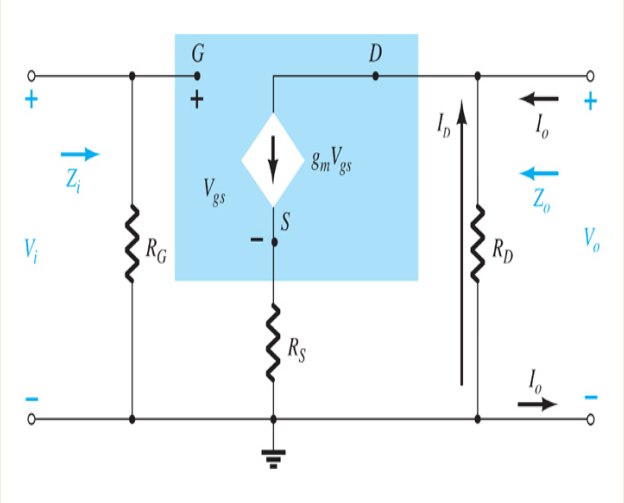
FET Transistors

AC Analysis (self bias)



$$Z_i = R_G$$

$$Z_o \cong R_D \Big|_{r_d \geq 10 R_D}$$

$$A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$$

$$A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S} \Big|_{r_d \geq 10(R_D + R_S)}$$

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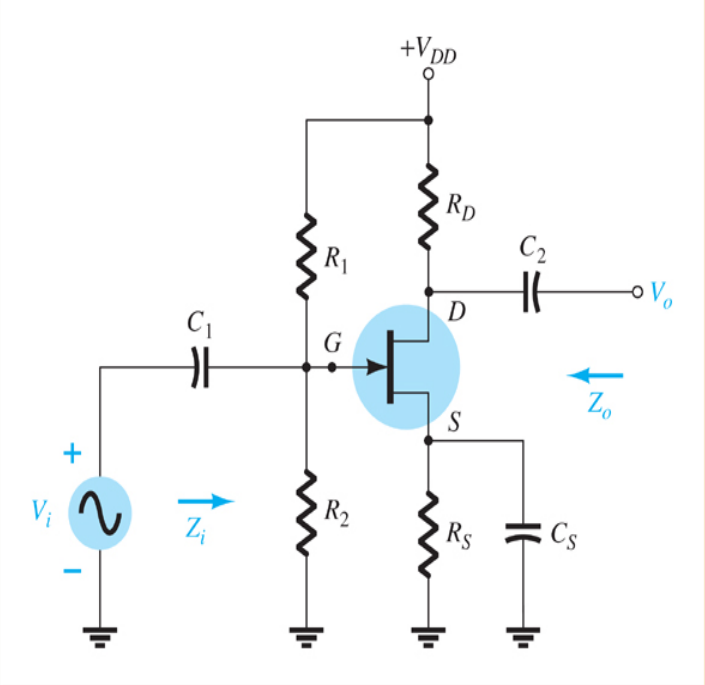
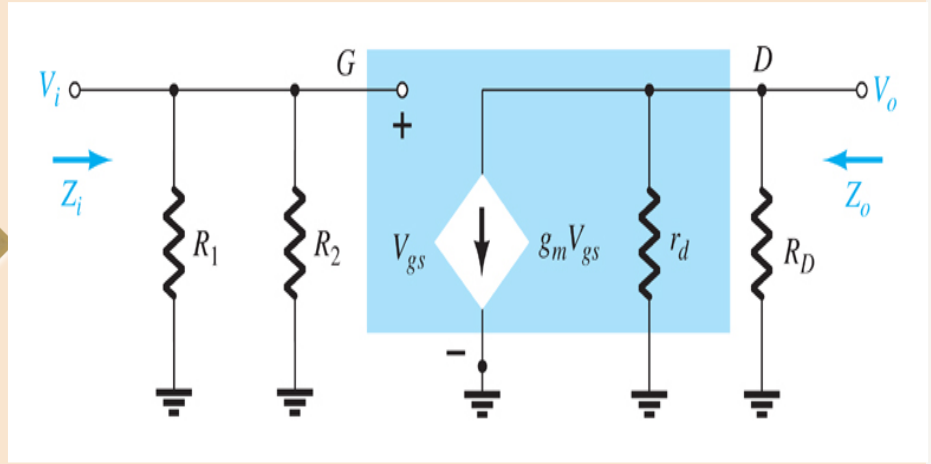
FET Transistors

AC Analysis (voltage divider)





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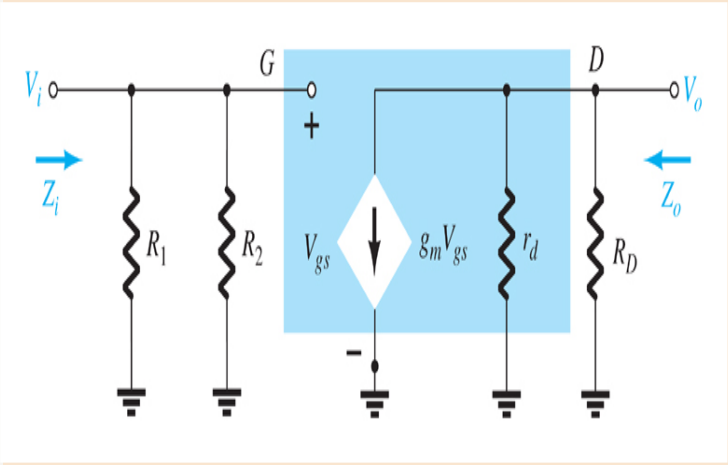
FET Transistors

AC Analysis (voltage divider)



$$Z_i = R_1 \| R_2$$

$$Z_o = r_d \| R_D$$

$$Z_o \cong R_D \Big|_{r_d \geq 10 R_D}$$

$$A_v = -g_m (r_d \| R_D)$$

$$A_v = -g_m R_D \Big|_{r_d \geq 10 R_D}$$

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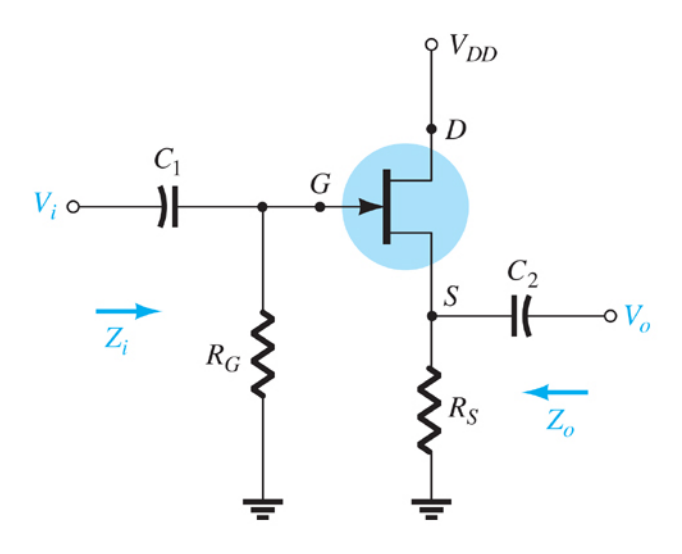
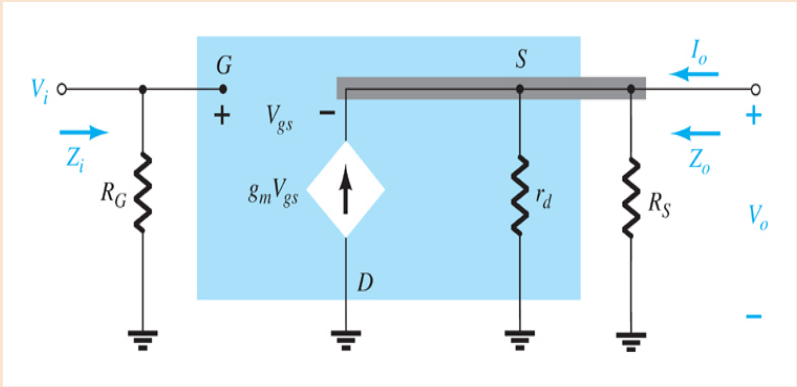
FET Transistors

Source Follower (Common-Drain)





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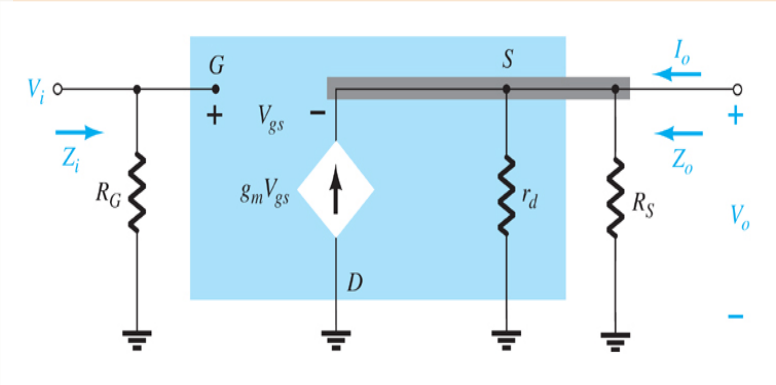
FET Transistors

Source Follower (Common-Drain)

$$Z_i = R_G$$



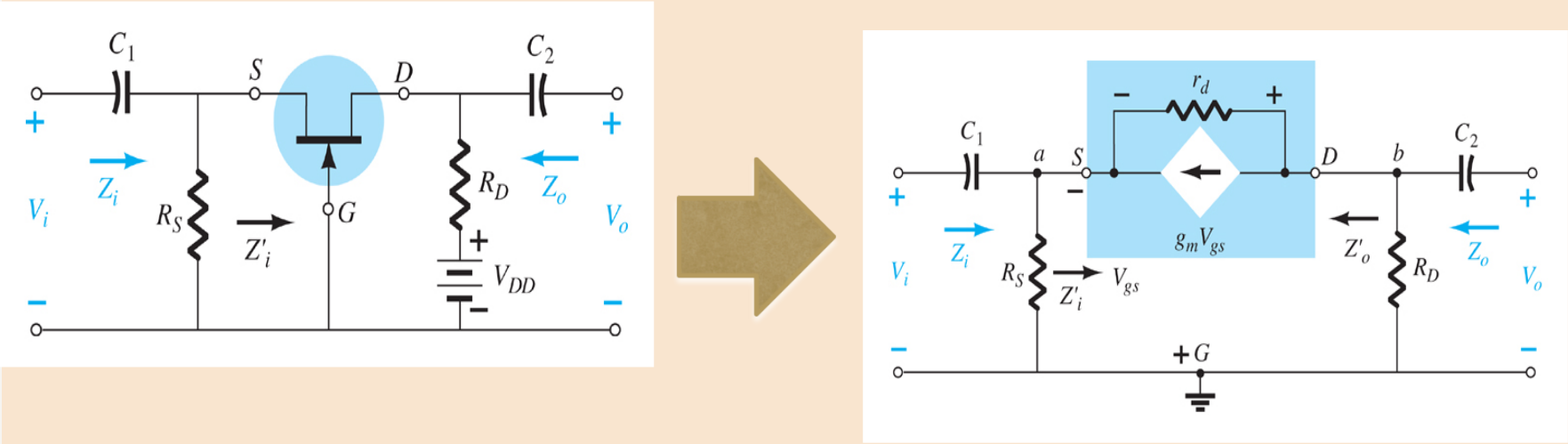
$$Z_o = r_d \| R_S \| \frac{1}{g_m}$$

$$Z_o \cong R_S \| \frac{1}{g_m} \Big|_{r_d \geq 10 R_S}$$

$$A_v = \frac{V_o}{V_i} = \frac{g_m (r_d \| R_S)}{1 + g_m (r_d \| R_S)} \qquad A_v = \frac{V_o}{V_i} = \frac{g_m R_S}{1 + g_m R_S} \Big|_{r_d \geq 10}$$

FET Transistors

Common-Gate (CG) Circuit



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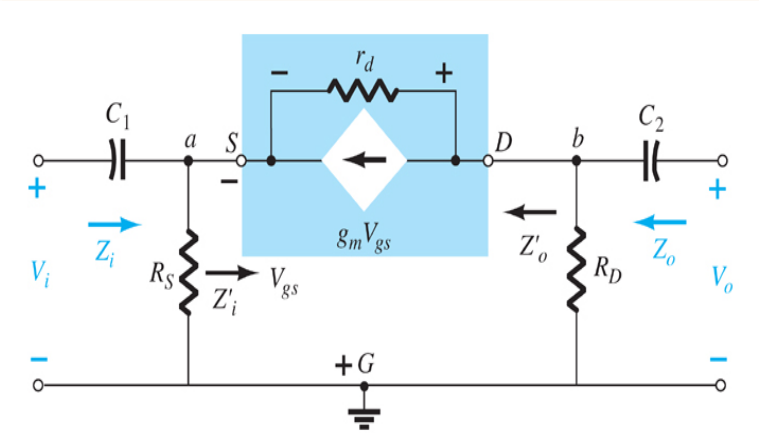
FET Transistors

Common-Gate (CG) Circuit



$$Z_i = R_S \| \left[\frac{r_d + R_D}{1 + g_m r_d} \right]$$

$$Z_i \cong R_S \| \frac{1}{g_m} \Big|_{r_d \geq 10 R_D}$$

$$Z_o = R_D \| r_d$$

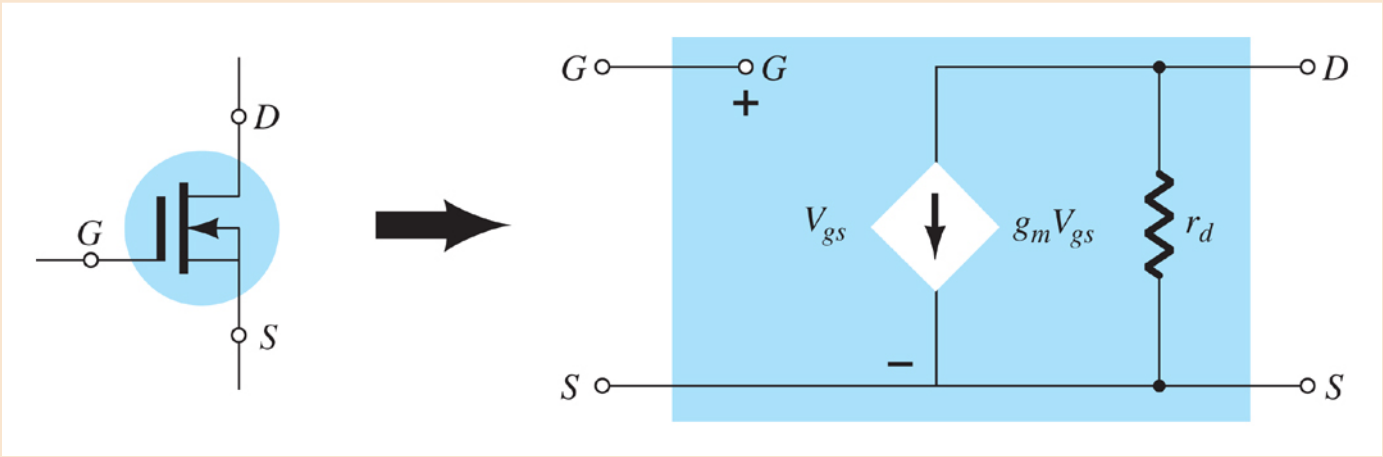
$$Z_o \cong R_D \Big|_{r_d \geq 10}$$

$$A_v = \frac{V_o}{V_i} = \frac{\left[g_m R_D + \frac{R_D}{r_d} \right]}{\left[1 + \frac{R_D}{r_d} \right]}$$

$$A_v = g_m R_D \Big|_{r_d \geq 10 R_D}$$

FET Transistors

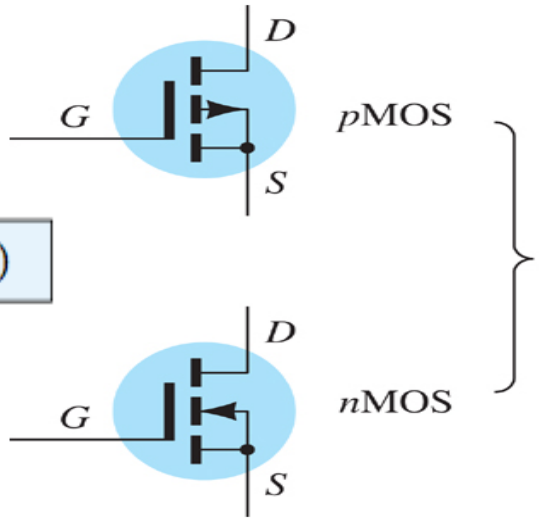
D-Type MOSFET AC Equivalent

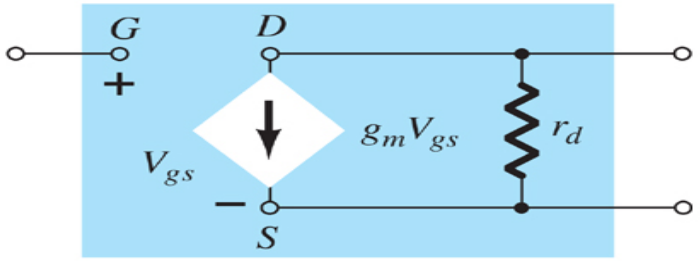


FET Transistors

Enhancement -Type MOSFET AC Equivalent

$$g_m = 2k(V_{GS_Q} - V_{GS(\text{Th})})$$





$$g_m = g_{fs} = |y_{fs}|\, r_d = \frac{1}{g_{os}} = \frac{1}{|y_{os}|}$$

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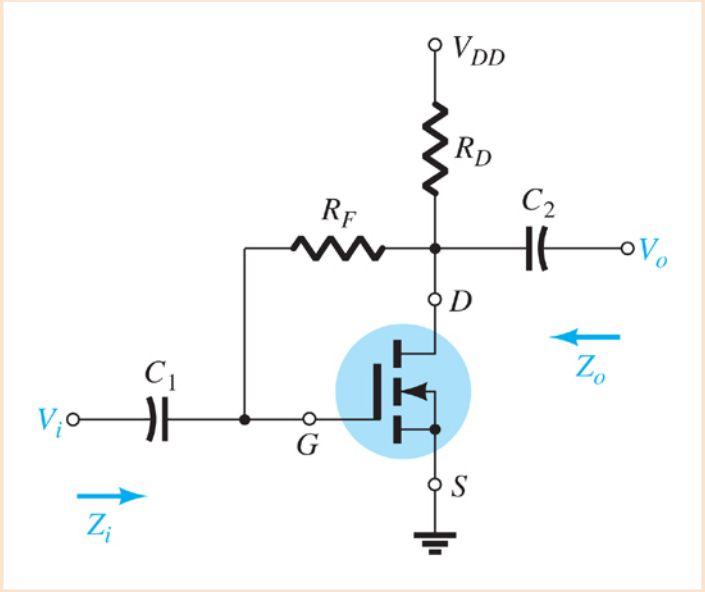
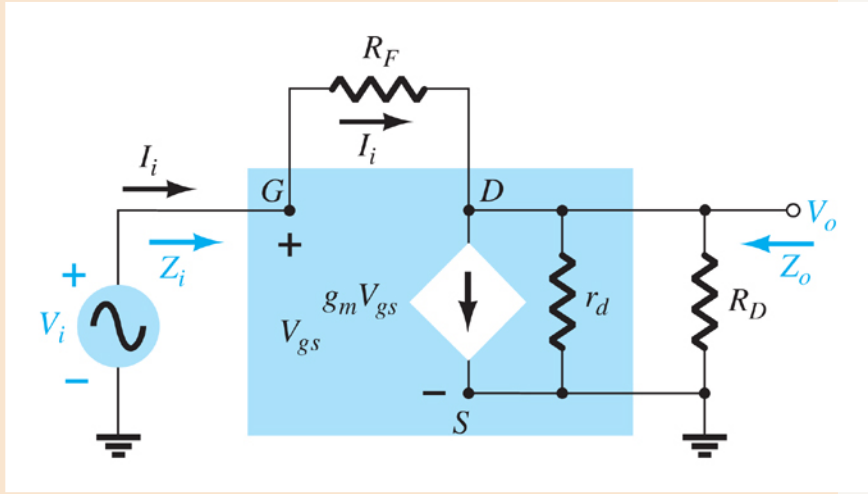
FET Transistors

Common-Source Drain-Feedback





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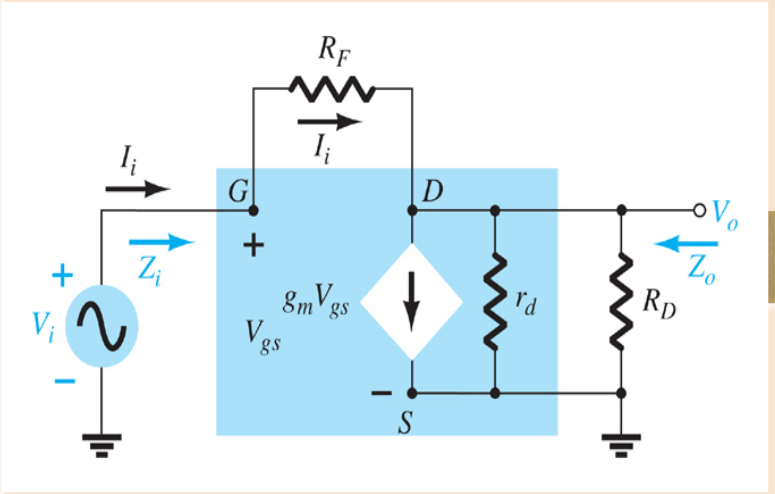
FET Transistors

Common-Source Drain-Feedback



$$Z_i = \frac{R_F + r_d \| R_D}{1 + g_m (r_d \| R_D)}$$

$$Z_i \cong \frac{R_F}{1 + g_m R_D} \Big|_{R_F >> r_d \| R_D,\, r_d \geq 10 R_D}$$

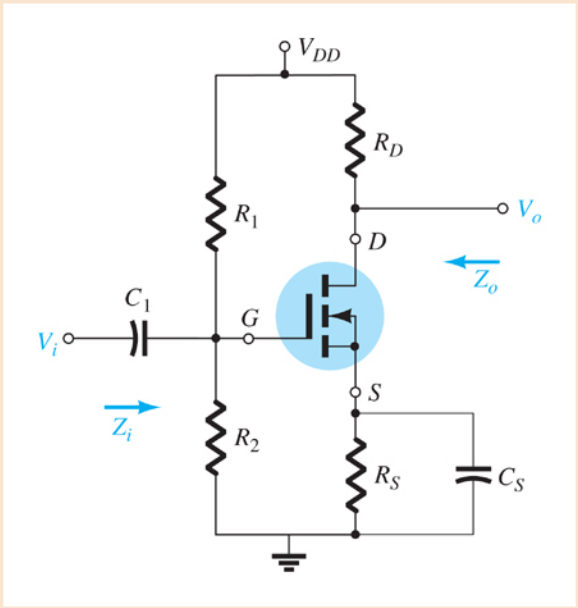
$$Z_o = R_F \| r_d \| R_D$$

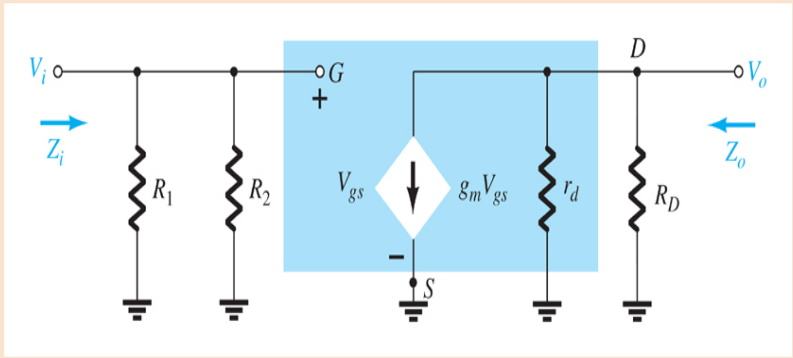
$$Z_o \cong R_D \Big|_{R_F >> r_d \| R_D,\, r_d \geq 10 R_D}$$

$$A_v = -g_m (R_F \| r_d \| R_D) \quad A_v \cong -g_m R_D \Big|_{R_F >> r_d \| R_D,\, r_d \geq 10 R_D}$$

FET Transistors

Common-Source Voltage-Divider Bias

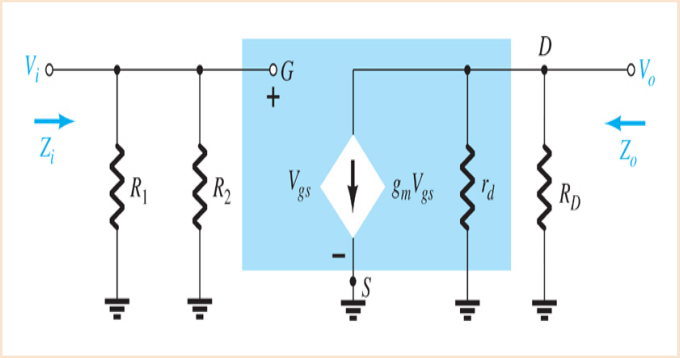




Dr.Hossam kasem
Electronics and Electrical Comm. Dept.

FET Transistors

Common-Source Voltage-Divider Bias



$$Z_i = R_1 \| R_2$$

$$Z_o = r_d \| R_D$$

$$Z_o \cong R_D \big|_{r_d \geq 10}$$

$$A_v = -g_m (r_d \| R_D) \qquad A_v \cong -g_m R_D \big|_{r_d \geq 10 R_D}$$

Questions